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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,604	10/28/2003	Mark W. Morgan	TI-36312	6318

23494 7590 12/03/2007

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
12/03/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/695,604	MORGAN ET AL.	
	Examiner	Art Unit	
	QUAN TRA	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-23,25 and 26* is/are rejected.

7)☒ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 10/5/07.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 21-23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art figure 2 in view of Fujioka (USP 6020781), previously cited.

Applicant's prior art figure 2 shows a multistage differential amplifier, comprising: a first amplifier stage (20), the first amplifier stage including a first differential pair of input transistors (102, 112) with loads (129, 131) coupled to a supply voltage (ground) through a first common-mode transistor (122) and a first pair of emitter-follower output transistors (140, 170) coupled to the first differential pair of input transistors; a second amplifier stage (40), the second amplifier stage including a second differential pair of input transistors (202, 212) coupled to the supply voltage through a second common-mode transistor (222) and a second pair of emitter-follower output transistors (240, 170) coupled to the second differential pair of input transistors, wherein the second differential pair of input transistors is coupled to the first pair of emitter-follower output transistors. The prior art figure 2 fails to teach the detail of circuit that generates Vbias. However, Fujioka's figure 1 shows a bias voltage generator (61-66) providing a stable constant voltage. Therefore, it would have been obvious to one having ordinary skill in the art to use Fujioka's bias voltage generator as the prior art figure 2's bias voltage generator for the purpose of providing a stable constant bias voltage. Thus, the modified prior art figure 2 further shows a voltage regulator coupled to control the first common-mode transistor, the voltage regulator

including (i) a differential amplifier (61) with a first input from a reference voltage, a second input from a temperature responsive unit (64-66), and an output to a third transistor connected between a supply voltage and the temperature responsive unit and a regulated voltage output locus between the third transistor (63) and the temperature responsive unit, wherein the temperature responsive unit includes in series a first resistor, a second resistor, and a diode-connected transistor.

As to claim 22, Fujioka fails to show that the diode connected transistor is connected between the first and second resistors. However, the function of Fujioka's voltage generator will not be changed of the positions of the diode connected transistor and the first resistor (65) are swap. Therefore, it would have been obvious to one having ordinary skill in the art to exchange the positions of the first resistor and the diode connected transistor due to the circuit equivalent function and dependent upon the environ of use to ensure optimum performance.

As to claim 23, Fujioka shows the diode-connected transistor is between the output locus and the first resistor, first resistor is between the diode-connected transistor and the second resistor, and the second resistor is between the first resistor and ground, and (ii) the input from a temperature responsive unit connects between the first resistor and the second resistor.

As to claim 25, the modified prior art figure 2 shows voltage regulator is coupled to control the second common-mode transistor.

As to claim 26, the prior art figure 1 further shows a third amplifier stage, having similar structure as the first and second amplifier stage, connected in series with the second amplifier stage.

Allowable Subject Matter

3. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 24 would be allowable because the prior arts fail to teach or suggest that the first differential pair of input transistors are NPN bipolar transistors, the first pair of emitter-follower output transistors are NPN bipolar transistors, the first common-mode transistor is a PMOS transistor, and the diode-connected transistor is an NPN bipolar transistor.

Response to Arguments

4. Applicant's arguments have been fully considered but they are not persuasive. Applicant argues that transistors 122 and 222 are current source, not common mode adjustments. The Examiner respectfully disagrees. Voltages at terminals 135, 137, 235 and 237 are determined by the currents generated by transistors 122 and 222. Thus, the common mode voltages are also determined by the currents generated by transistors 122 and 222. Thus, 122 and 222 are considered as common mode adjustments.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/QUAN TRA/
PRIMARY EXAMINER
Art Unit 2816